



INTEL

Omni97 Status Review

C. Stone

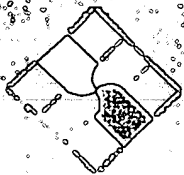
Property Information



XYLAN

Status

- ✓ CAM design complete
- ✓ Initial fabric modelling complete
- ✓ Fabric requirements defined, verilog in progress
- ✓ Quotes in hand for CAM and Fabric ASICS
- ✓ LED Module quoted
- ✓ PRD in progress



Xylan

Cam

✓ 48 bit compares

✓ 1024 entries, cascadable

✓ Integrated RMON support

✓ Compare possible every 2 clocks @ 80MHz

□ Working to improve to 1 clock

✓ Atmel

□ \$9.38

□ \$220K NRE

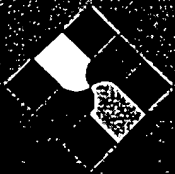
✓ LSI Logic

□ \$10.32

□ \$130K NRE

Proprietary Information

G. Stone



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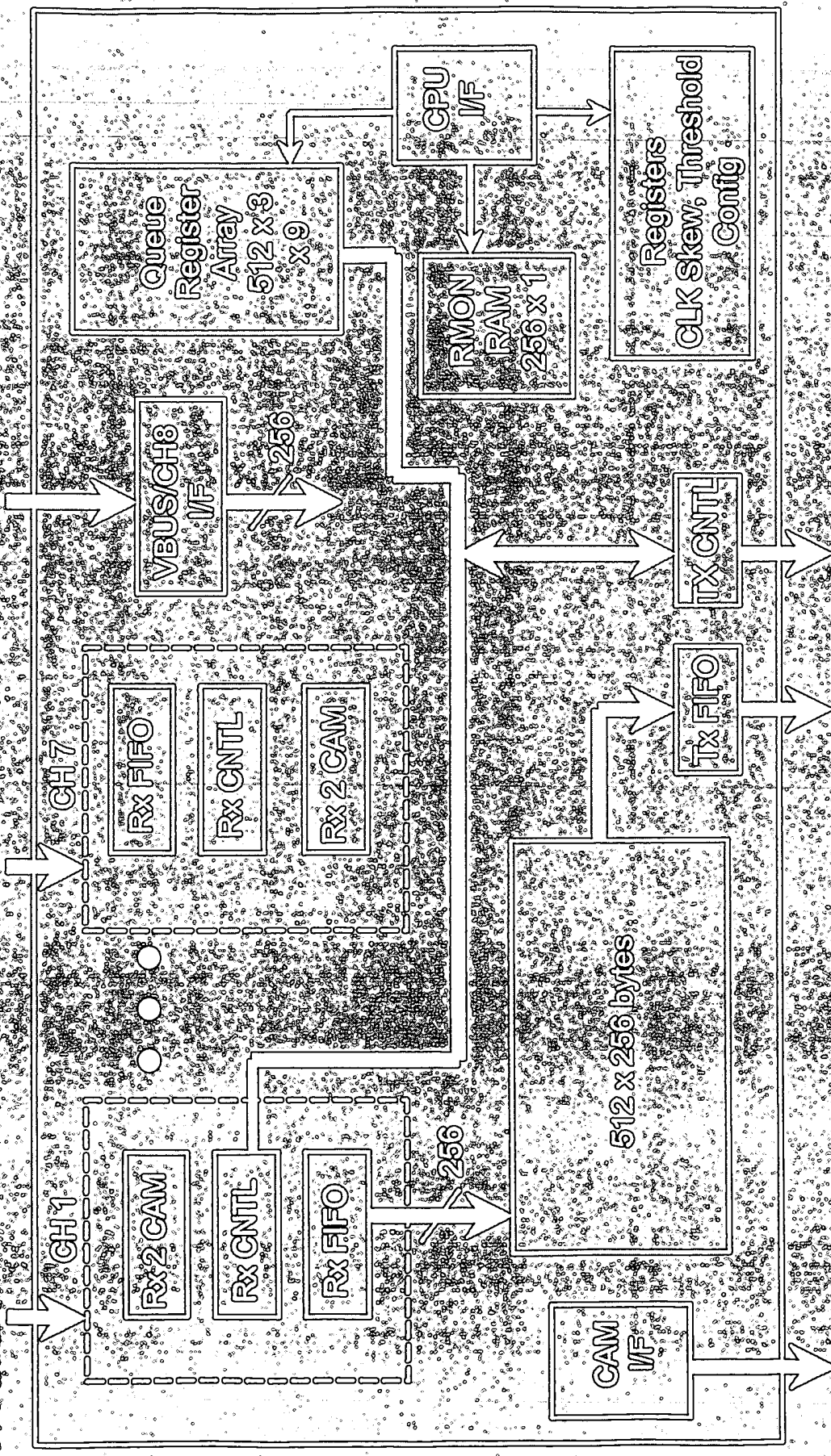
Fabric

- ✓ 8 - 1.28 Gigabit links
- ✓ 17+ million frames/sec sustained
- ✓ 2+ Million frames/sec per link
 - 14 ports @ 100Mbps wire-speed
- ✓ VBUS format
- ✓ 640/960 Mbps VBUS, receive only
- ✓ Quote from LSI - \$79.94, \$195K NRE



Fabric ASIC Block Diagram

XILINX





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LED Module

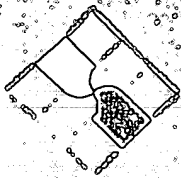
✓ 4 x 9 Array of green LEDs

✓ 1.64" x .79" x .2"

✓ Quote from Siemens

☐ \$9.25 - 25k pieces

☐ \$57K NRE



XYLIN

Ethernet modules planned

✓ 8 x 100 Mbps Full Duplex

✓ 16 x 100 Mbps

✓ 24 x 100 Mbps

□ 32 ports, if LED module works out

✓ 32 x 10 Mbps

✓ 2 x 1000 Mbps



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Cost Targets - Burdened

Board

List/Port

8 x 100BaseFx

\$1600

\$1000

16 x 10/100

\$900

\$280

32 x 10/100

\$1200

\$190

32 x 10

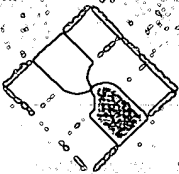
\$950

\$148

Gigabit Ethernet

\$1600?

\$4000



XYLEM

Other Modules

✓ 2 x OC-12

✓ MPM



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Schedule

- ✓ ASICs in-house [redacted]
- ✓ First shipments [redacted]
- ✓ Currently about 2 weeks ahead

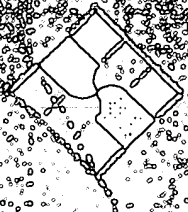


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Issues

✓ May need to add cost to achieve wire-speed on 16-port module

- ❑ Mammoth may not have enough SDRAM bandwidth
- ❑ Would increase cost/port by about \$8, or about \$50/list



XILANI

Next steps

- ✓Negotiate for lower NREs
- ✓Select CAM and Fabric vendors
- ✓Issue purchase orders
- ✓Complete PRD



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